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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/849,162	05/04/2001	David E. Zeidler	80113-0122 (D2382)	9802

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RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER
TRAN, TRANG U

ART UNIT	PAPER NUMBER
2614	2

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/849,162	ZEIDLER ET AL.	
	Examiner	Art Unit	
	Trang U. Tran	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9, 11-23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Srivastava (US Patent No. 5,184,091).

In considering claim 1, Srivastave discloses all the claimed subject matter, note 1) the claimed an oscillator that generates the clock signal is met by the VCO 104 of the phase lock loop 28 (Fig. 3, col. 7, lines 8-47), 2) the claimed a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock is met by the phase lock loop 28 (Fig. 3, col. 7, lines 8-47), and 3) the claimed a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range is met by the static phase error corrector 29 which includes threshold detector 60 coupled to output 58 of error amplifier 55 and having a pair of outputs 61 and 62 (Fig. 3, col. 7, line 48 to col. 8, line 10 and col. 14, line 60 to col. 16, line 64).

In considering claim 2, the claimed wherein the frequency range bounder includes an output multiplexer and a threshold register that stores at least one threshold

value and that is coupled to the output multiplexer, wherein the output multiplexer receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to the selected range is met by the threshold detector 60 and the multiplexer 123 (Fig. 3, col. 14, line 32 to col. 16, line 21).

In considering claim 3, the claimed wherein said at least one threshold register that stores at least one threshold value is a high limit register that stores an upper value and a low limit register that stores a lower value is met by the threshold detector 60 and the multiplexer 123 (Fig. 3, col. 14, line 32 to col. 16, line 21).

In considering claim 4, the claimed wherein the frequency range bounder includes an output multiplexer that selects one of the upper value, the control signal, and the lower value as the bounded control signal and outputs the bounded control signal to the oscillator to bound the oscillator frequency between an upper level and a lower level is met by the threshold detector 60 and the multiplexer 123 (Fig. 3, col. 14, line 32 to col. 16, line 21).

In considering claim 5, the claimed wherein the frequency range bounder includes at least one of a high comparator and a low comparator coupled to the output multiplexer, wherein the high comparator compares the control signal with a high limit and the low comparator compares the control signal with a low limit, and wherein the output multiplexer outputs the upper value as the bounded control signal if the control signal is above the high limit and outputs the lower value as the bounded control signal if the control signal is below the low limit is met by the threshold detector 60, the limit

detector 70 which responds to the output count of counter 63 and compares the output count to predetermined high and low count limits and the multiplexer 123 (Fig. 3, col. 14, line 32 to col. 16, line 21).

In considering claim 6, the claimed wherein the frequency range bounder includes at least one of a minimum function block coupled to the high limit register and a maximum function block coupled to the low limit register, wherein the minimum function block outputs the smaller of the control signal and the upper value and wherein the maximum function block outputs the larger of the control signal and the lower value as the bounded control signal is met by the frequency maxima and frequency minima signals are applied to horizontal frequency detector 180 (Fig. 3, col. 10, line 48 to col. 13, line 2).

In considering claim 7, the claimed wherein the frequency range bounder includes a comparator coupled to the high limit register and low limit register, wherein the comparator compares the control signal with the upper and lower values and outputs the control signal to the output register if the control signal is between the upper and lower values is met by the threshold detector 60, the limit detector 70 which responds to the output count of counter 63 and compares the output count to predetermined high and low count limits and the multiplexer 123 (Fig. 3, col. 14, line 32 to col. 16, line 21).

In considering claim 8, the claimed wherein the frequency range bounder includes an output register coupled to the comparator, and wherein the comparator compares the control signal by comparing data values in the control signal with the

upper and lower values and latching the data values in between the upper and lower values into tile output register is met by the threshold detector 60, the limit detector 70 which responds to the output count of counter 63 and compares the output count to predetermined high and low count limits and the multiplexer 123 (Fig. 3, col. 14, line 32 to col. 16, line 21).

In considering claim 9, the claimed further comprising a drive circuit that receives the bounded control signal and that drives the oscillator in accordance with the bounded control signal is met by the control signal applied to voltage controlled oscillator 104 is the combination of inputs 101 and discloses all the claimed subject matter, note 1) the claimed and therefore, changes at input discloses all the claimed subject matter, note 1) the claimed causes corresponding changes of frequency of voltage controlled oscillator 104 (col. 15, line 66 to col. 16, line 64).

In considering claim 11, the claimed wherein the incoming video signal is an analog signal and the clock signal portion of the incoming video signal is at least one of horizontal and vertical timing information embedded in the incoming video signal is met by the sync signal separator 30 (Fig. 2, col. 4, line 10 to col. 5, line 32).

Claim 12 is rejected for the same reason as discussed in claims 1 and 2.

Claims 13-19 are rejected for the same reason as discussed in claims 2-8, respectively.

Claim 20 is rejected for the same reason as discussed in claim 1.

In considering claim 21, the claimed further comprising the step of outputting a bounded control signal from the frequency range bounder to the oscillator to conduct the limiting step.

Claims 22-23 are rejected for the same reason as discussed in claims 4-5, respectively.

Claim 25 is rejected for the same reason as discussed in claim 11.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava (US Patent No. 5,184,091) in view of Leske (US Patent No. 5,473,385).

In considering claim 10, Srivastava discloses all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein the incoming video signal is a digital signal and the clock signal portion of the incoming video signal is program clock reference data for the digital signal. Leske teaches that the MPEG standards provide for a MPEG transport packet stream that includes encoded video data and that also includes ten encoder clock signals per second in the form of "program clock reference" (PCR) structures, one of which is indicated by reference numeral 25 (Fig. 1, col. 3, lines 8-38). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the program

clock reference data for the digital signal as taught by Leske into Srivastava's system in order to adjust a decoding clock to accommodate mismatches between its frequency and the frequency of an encoding clock in response to video synchronization signals in the digital video signal.

Claim 24 is rejected for the same reason as discussed in claim 10.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Murayama et al. (US Patent No. 6,396,354 B1) disclose PLL detection circuit with lock judgement circuit.

Hasegawa (US Patent No. 6,133,770) discloses phase locked loop circuit.

Onagawa (US Patent No. 5,657,089) discloses video signal processing device for sampling TV signals to produce digital data with interval control.

Soda (US Patent No. 5,956,378) discloses phase lock by a frequency and phase difference between input and VCO signals with a frequency range adjusted by synchronism between the input and the VCO signals.

Walker et al. (US Patent No. 5,579,348) disclose method and apparatus for improving the apparent accuracy of a data receiver clock circuit.

Knechtel (US Patent No. 4,933,959) discloses tracking bit synchronizer.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Trang U. Tran** whose telephone number is **(703) 305-0090.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John W. Miller,** can be reached at **(703) 305-4795.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

TT TT
August 19, 2003

MICHAEL H. LEE
PRIMARY EXAMINER